SUPERJUNCTION DEVICE WITH ADDED CHARGE AT TOP OF PYLONS TO INCREASE RUGGEDNESS

RELATED APPLICATION

[0001] The present application is based on and claims benefit of U.S. Provisional Application Ser. No. 60/417,212, filed October 8, 2002, entitled SUPERJUNCTION DEVICE WITH ADDED CHARGE AT TOP OF P PYLONS TO INCREASE RUGGEDNESS, to which a claim of priority is made.

FIELD OF THE INVENTION

[0002] This invention relates to superjunction semiconductor devices and more specifically to the improvement of the ruggedness of such devices without substantially reducing the breakdown voltage of the device.

BACKGROUND OF THE INVENTION

[0003] Superjunction devices are well known in which a plurality of spaced, parallel columns or pylons of one conductivity type extend though a portion or all of the thickness of a wafer of the other conductivity type. The pylons are P type for an N channel device, which is the example to be used herein. The pylons are then capped at their tops with a MOSgated structure which, when turned on, permits vertical current flow through the N body of the wafer. The total charge of the pylons is matched to that of the surrounding N body so that, in reverse bias, the P pylons and the N body fully deplete to block voltage across the thickness of the wafer.

[0004] It is known that avalanche current may flow in such devices under reverse bias. This avalanche current flows into the channel region and under the source regions of the MOSgated structures (the R_b[1] region of the device) and then to the source metal. If the horizontal portion of the avalanche current, hence, the

voltage drop across the source - P body junction, is high enough, it can turn on the parasitic transistor in the MOS structure.

[0005] The horizontal portion of the avalanche current can be reduced by increasing the charge in the P pylons and overbalancing the P regions (no charge balance), thus making the device less susceptible to avalanche current turn-on. However, the increased pylon concentration reduces breakdown voltage since the P pylons are not fully depleted during reverse bias.

[0006] Thus, the design trade-off between device ruggedness (avalanche energy) and breakdown voltage is complicated.

[0007] In other words, to achieve both high breakdown voltage and high avalanche energy is a critical technique in the design of superjunction type of devices. When a superjunction device works with a perfect charge balance condition, it can support high reverse bias voltage. However, the large amount of the horizontal avalanche current through the R_b^1 will easily trigger the bipolar structure in the MOSFET device. On the other hand, when the device works with a higher, and unbalanced p-charge in the pylons, avalanche energy is usually high, but with a low breakdown voltage.

BRIEF DESCRIPTION OF THE INVENTION

[0008] In accordance with the invention, only a small portion at the top of each pylon has an increased charge and thus is charge-unbalanced relative to its surrounding oppositely charged region.

[0009] A device according to the invention produces a favorable trade-off of breakdown voltage and avalanche energy. When only the top of the pylon receives a higher dose implant relative to its lower portion, the device can still withstand a high breakdown voltage. When the device is avalanched, the avalanche current is uniform at the lower portion of the device and starts to converge toward each pylon when it flows close to the top of the device. This keeps the avalanche current away from the R_b^1 region so that the device can hold a much higher avalanche energy.

[0010] In the preferred embodiment, 25% of the top portion of each pylon has an increased charge, and the remainder of each pylon has a balanced charge relative to its surrounding region. Also, preferably, the charge increase at the top of each pylon is about 15 to 20% greater than that of the remainder of its body. As a result, the preferred embodiment exhibits a favorable combination of breakdown voltage and avalanche energy. It should be noted that the values stated herein may be modified to obtain the desired tradeoff between the various characteristics of the device such as its ruggedness and its breakdown voltage rating.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a cross-section of a superjunction wafer which includes the features of the invention.

[0012] Figure 2 is a cross-section of Figure 1 taken across section line 2-2 in Figure 1.

[0013] Figure 3 schematically illustrates the operation of the invention for a single pylon of Figures 1 and 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0014] Figures 1 and 2 show a small portion of a superjunction MOSFET device of well-known construction which is modified in accordance with the invention as will be described.

[0015] The device is formed in a silicon wafer 10 (the term wafer is used interchangeably with chip or die) which has a main substrate portion 11, shown as highly doped (N^{++}) silicon. (Figures 1 and 2 show an N channel device. All conductivity types can be reversed to produce a P channel device.)

[0016] The superjunction concept includes the use of a plurality of spaced P type "pylons" 20, 21, 22 which extend vertically upward toward the upper surface of wafer 10. Conventionally, these pylons have a P concentration such that their total charge equals the total charge in the surrounding N type body 23 (usually an

epitaxially deposited layer) of silicon above the substrate 11. In this way, during reverse bias, the P type pylons and N type body fully deplete to block voltage. However, the N type concentration in region 23 can be higher than that used for the conventional MOSFET so the device has a much lower on resistance when turned on.

[0017] A MOSgated structure is also provided in the usual manner, and is shown as P^- channel regions 30, 31, 32 which receive N^+ source regions 33, 34, 35 respectively, which may be annular regions. The P^- regions in channels 30, 31 and 32 which are below the sources 40, 41 and 42 respectively are the R_b' regions through which avalanche current can flow.

[0018] A gate oxide 40 overlies the invertible channel regions between the source regions and respective channel regions and a polysilicon gate electrode 41 overlies the gate oxide 40. An insulation layer 42 such as LTO overlies and insulates the polysilicon gate segments of gate 41 from an overlying source electrode 43. A drain contact 50 is connected to the bottom of wafer 10.

[0019] The pylons 20, 21 and 22 can be made in any desired way. One conventional process includes the sequential epitaxial deposition of N type layers 60 to 65, with aligned P type diffusions following the formation of each layer to form the final pylon. The number of layers and their thickness and concentrations are well-known. Typically, for a high voltage device, six layers will be used to get the needed length.

[0020] In accordance with the invention, the top portion of each of the pylons (and the diffusion in the top-most layer 65) has a greater concentration P_2 than that of the remaining portion of the column in which each diffusion has the concentration P_1 wherein $P_1 < P_2$.

[0021] Note that the length of the pylon portion having an increased concentration is preferably less than about 25% (and is about 16% in the embodiment shown) of the full pylon length. Further, the concentration P_2 is preferably about 15 to 20% greater than P_1.

[0022] Figure 3 shows the pylons 20 and shows the manner in which the heavier doped portion of the pylon or P column 20 improves the device operation.

[0023] Thus, achieving both high breakdown voltage and high avalanche energy is the aim of the critical design of superjunction type of device. When a superjunction works at perfect charge balance condition, it can support high reverse bias voltage between electrode 43 and 50 (Figure 1). However, a large avalanche current through the R_b^1 will easily trigger the bipolar structure in the MOSFET device section. On the other hand, when the device works with a higher p-charge in the pylon, avalanche energy is usually high, but with a reduced breakdown voltage.

[0024] This invention improves the trade-off of breakdown voltage and avalanche energy. Thus, when only top of the p-column 20 receives a higher dose implant P_2 (than that of the lower portion of the p-column), the device still can withstand a relatively high breakdown voltage. When the device is avalanched, however, the avalanche current, as shown by arrows in Figure 3, is uniform at the lower portion of the device but starts to converge toward the p-column close to top of the device. This keeps the avalanche current away from the R_b' region under source 33 so that the device can handle a much higher avalanche energy.

[0025] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.